1. A data processing device comprising:

a central processing unit (CPU); and

a digital signal processing unit whose operation is controlled by the CPU decoding instructions, the CPU and the digital signal processing unit being mounted on a single semiconductor substrate;

the digital signal processing unit including:

a register holding fixed-point data;

an addition/subtraction circuit for processing fixed-point data; and

a multiplication circuit for processing fixed-point data.

2. A data processing device according to claim 1, wherein when a first instruction is executed to transfer data, whose bit length is shorter than the bit length of the register, from outside the digital signal processing unit to the register, the digital signal processing unit inputs the data justified to the higher-order side of the register and enters zero at a redundant lower-order side of the register, and when a second instruction is executed to transfer data, whose bit length is shorter than the bit length of the register, from the register to the outside of the digital signal processing unit, the digital signal processing unit outputs a required bit length of the data from the higher-order side of the register to the outside.

3. A data processing device according to claim 2, further comprising:

first, second and third address buses through which addresses are transferred from the CPU;

a first memory connected to the first and second address buses;

a second memory connected to the first and third address buses;

a first data bus connected to the first and second memories, the CPU and the digital signal processing unit;

a second data bus connected to the first memory and the digital signal processing unit; and

a third data bus connected to the second memory and the digital signal processing unit.

4. A data processing device comprising:

a first processing unit having a first register and a first calculator, the first calculator performing calculation on data contained in the first register; and

a second processing unit having a second register and a second calculator, the second calculator performing calculation on data contained in the second register;

wherein the first processing unit processes integer data and the second processing unit processes fixed-point data.

5. A data processing device according to claim 4, wherein

when a first instruction is executed to transfer data, whose bit length is shorter than the bit length of the first register, from outside the first processing unit to the first register, the first processing unit inputs the data justified to the lower-order side of the first register and extends and inputs the most significant bit value of the data to the redundant higher-order side of the first register;

when a second instruction is executed to transfer data, whose bit length is shorter than the bit length of the first register, from the first register to the outside of the first processing unit, the first processing unit outputs a required bit length of the data from the lower-order side of the first register;

when a third instruction is executed to transfer data, whose bit length is shorter than the bit length of the second register, from outside the second processing unit to the second register, the second processing unit inputs the data justified to the higher-order side of the second register and inputs zero to the redundant lower-order side of the second register; and

when a fourth instruction is executed to transfer data,

whose bit length is shorter than the bit length of the second register, from the second register to the outside of the second processing unit, the second processing unit outputs a required bit length of the data from the higher-order side of the second register.

6. A data processing device according to claim 5, wherein the first processing unit is a central processing unit and the second processing unit is a digital signal processing unit.

7. A data processing device according to claim 6, being formed on a single semiconductor substrate.

8. A data processing device comprising:

a register; and

a calculator performing calculation on data contained in the register;

wherein when a first instruction is executed to transfer data, whose bit length is shorter than the bit length of the register, from outside the data processing device to the register, the data processing device inputs the data justified to the higher-order side of the register and inputs zero to the redundant lower-order side of the register, and when a second instruction is executed to transfer data, whose bit length is shorter than the bit length of the register, from the register to the outside of the data processing device, the data processing device outputs a required bit length of the data from the higher-order side of the register.

9. A data processing device according to claim 8, wherein the first and second instructions are instructions that handle fixed-point data.

10. A data processing device according to claim 9, having installed outside it:

a central processing device connected to the data processing device through a first data bus;

a first memory connected to the data processing device through a second data bus; and

a second memory connected to the data processing device through a third data bus.

11. A data processing device according to claim 10, wherein the data processing device, the central processing device and the first and second memories are formed on a single semiconductor substrate.

12. A data processing device comprising:

a central processing unit having a calculation circuit for executing an arithmetic operation or a logic operation;

first, second and third address buses to which addresses are selectively transferred from the central processing unit;

a first memory connected to the first and second address buses and accessed by the address from the central processing unit;

a second memory connected to the first and third address buses and accessed by the address from the central processing unit;

a first data bus connected to the first and second memories and the central processing unit and through which data is transferred;

a second data bus connected to the first memory and through which data is transferred;

a third data bus connected to the second memory and through which data is transferred; and

a digital signal processing unit connected to the first, second and third data buses and adapted to operate in synchronism with the central processing unit;

wherein the digital signal processing unit includes:

an addition/subtraction circuit forprocessing fixed-point data; and

a multiplication circuit for processingfixed-point data.

13. A data processing device according to claim 12, wherein

the central processing unit further includes a first

register file for holding data necessary for calculation and a result of calculation;

the digital signal processing unit further includes a second register file for holding data necessary for processing and a result of processing;

a means for inputting data, whose bit length is shorter than the bit length of the first register file, from the first data bus justified to the lower- order side of one of registers in the first register file and for extending and inputting the most significant bit value of the data to the redundant higher-order side of the register;

a means for outputting a required bit length of data, whose bit length is shorter than the bit length of the first register file, from the lower-order side of one of registers in the first register file to the first data bus;

a means for inputting data, whose bit length is shorter than the bit length of the second register file, from one of the first, second and third data buses justified to the higher-order side of one of registers in the second register file and for inputting zero to the redundant lower-order side of the register; and

a means for outputting a required bit length of data, whose bit length is shorter than the bit length of the second register file, from the higher-order side of one of registers in the second register file to one of the first, second and third data buses.

14. A data processing device according to claim 12, wherein an instruction calling for execution of an integer data calculation and an instruction calling for execution of a fixed-point data calculation are provided separately.

15. A data processing device according to claim 12, wherein an instruction calling for execution of an integer data transfer and an instruction calling for execution of a fixed-point data transfer are provided separately.

16. A data processing device according to claim 13,

wherein an instruction calling for execution of an integer data transfer and an instruction calling for execution of a fixed-point data transfer are provided separately.

17. A data processing device according to claim 12, being formed on a single semiconductor substrate.

18. A data processing device according to claim 13, being formed on a single semiconductor substrate.

19. A data processing device comprising:

a multiplier for inputting a multiplier and a multiplicand and outputting a result of multiplication of the multiplier and the multiplicand; and

a shifter for shifting the output of the multiplier;

wherein when integer data is multiplied, the shifter outputs the output of the multiplier without shifting it, and when fixed-point data is multiplied, the shifter shifts left the output of the multiplier by one bit and inputs zero to the least significant bit.

20. A data processing device according to claim 19, wherein an instruction calling for execution of an integer data calculation and an instruction calling for execution of a fixed-point data calculation are provided separately.

21. A data processing device according to claim 20, further comprising:

an arithmetic and logic calculator; and

a register for holding data to be calculated in the multiplier and the arithmetic and logic calculator and the calculation results.